CLAIMS

1. A multi-channel integrated circuit comprising:

a plurality of on-chip channels,

a digital-to-analogue converter (DAC) located in each channel, each DAC having an analogue output,

an on-chip digital input port for receiving digital data,

an on-chip interface and control logic circuit for receiving digital data from the digital input port and for selectively applying the digital data to the DACs for conversion thereof to analogue output signals,

an on-chip monitoring output terminal, and

an on-chip switch network coupled to the on-chip monitoring output terminal and to the analogue outputs of at least some of the DACs, the switch network being operable under the control of the interface and control logic circuit for selectively switching the analogue output signals from the at least some of the DACs to the monitoring output terminal for facilitating external monitoring thereof.

2. A multi-channel integrated circuit as claimed in Claim 1 in which the analogue output of each DAC is coupled to the switch network.

3. A multi-channel integrated circuit as claimed in Claim 1 in which each on-chip channel of the plurality of on-chip channels terminates in a corresponding on-chip analogue output terminal for outputting the analogue output signal from the corresponding DAC.

4. A multi-channel integrated circuit as claimed in Claim 1 in which at least one on-chip analogue input terminal is provided for receiving a corresponding analogue input signal, each analogue input terminal being coupled to the switch network, and the switch network is operable under the control of the interface and control logic circuit for selectively switching each analogue input signal to the monitoring output terminal.

5. A multi-channel integrated circuit as claimed in Claim 4 in which a plurality of analogue input terminals are provided, each of which are coupled to the switch network for receiving respective analogue input signals.

6. A multi-channel integrated circuit as claimed in Claim 4 in which the switch network is operated under the control of the interface and control logic circuit for sequentially switching the analogue output signals from the DACs and the analogue input signals from the analogue input terminals to the monitoring output terminal.

7. A multi-channel integrated circuit as claimed in Claim 1 in which the interface and control logic circuit is responsive to an externally generated control signal applied through the input port for operating the switch network.

8. A multi-channel integrated circuit as claimed in Claim 1 in which the switch network is provided by a multiplexer.

9. A multi-channel integrated circuit as claimed in Claim 1 in which a DAC register is located in each on-chip channel for sequentially receiving digital data words from the input port under the control of the interface and control logic circuit for loading into the corresponding DAC for conversion thereof.

10. A multi-channel integrated circuit as claimed in Claim 1 in which correction code registers are provided corresponding to at least some of the respective DACs for storing respective correction codes for correcting for offset errors in the corresponding DACs, and corresponding adding means are provided for adding the correction codes to digital data words to be converted by the corresponding DACs.

11. A multi-channel integrated circuit as claimed in Claim 10 in which each correction code register is programmable.

12. A method for monitoring respective analogue output signals from at least some of a plurality of on-chip DACs located in respective on-chip channels of a multi-channel integrated circuit, the method comprising the steps of:

providing an on-chip monitoring output terminal in the integrated circuit for sequential monitoring of the analogue output signals from the at least some of the DACs,

providing an on-chip switch network for selectively coupling analogue

outputs of the at least some of the DACs to the monitoring output terminal for selectively applying the analogue output signals from the DACs to the monitoring output terminal,

providing an on-chip interface and control logic circuit for controlling the switch network for selectively switching the analogue output signals to the monitoring output terminal, and

reading the analogue output signals from the monitoring output terminal.

13. A method as claimed in Claim 12 in which an on-chip input port is provided for inputting an externally generated control signal to the interface and control logic circuit for controlling the operation of the switch network.

14. A method as claimed in Claim 12 in which the method further comprises providing at least one on-chip analogue input terminal for receiving a corresponding analogue input signal, coupling each analogue input terminal to the switch network, and operating the switch network under the control of the interface and control logic circuit for selectively switching the analogue input signal on each analogue input terminal to the monitoring output terminal for monitoring thereof.

15. A method as claimed in Claim 14 in which a plurality of analogue input terminals are provided for receiving respective analogue input signals.

16. A method as claimed in Claim 14 in which the analogue output signals from the respective DACs and the analogue input signals from the respective analogue input terminals are sequentially switched by the switch network to the monitoring output terminal.

17. A method as claimed in Claim 14 in which the method further comprises the step of applying analogue input signals to the respective analogue input terminals.

18. A method as claimed in Claim 12 in which a plurality of on-chip analogue output terminals are provided, one on-chip analogue output terminal being provided for each on-chip channel for outputting the analogue output signals of the respective DACs independently of each other.

19. A method as claimed in Claim 12 in which the method further comprises the step of selectively applying digital data to the respective DACs through the on-chip digital input port under the control of the interface and control logic circuit for conversion thereof to analogue output signals.

20. A method as claimed in Claim 12 in which the method further comprises providing correction code registers corresponding to at least some of the respective DACs for storing respective correction codes for correcting for offset errors in the corresponding DACs, and providing corresponding adding means for adding the correction codes to digital data words to be converted by the corresponding DACs.

21. A method as claimed in Claim 20 in which each correction code register is programmable.